ECE 230 – DIGITAL SYSTEMS HOMEWORK

**FALL 2010**

8/23/2010: none  
8/25/2010: [homework 1](http://coen.boisestate.edu/smloo/files/2011/09/hwk-8-25-2010.pdf)

8/27/2010: 2.6, 2.9, 2.13, 2.14, 2.31

*Total possible points 85 points*

8/30/2010 (*Due: 9/8*): 2.10, 2.11, 2.24, 2.25, 2.34, 2.37  
9/1/2010 (*Due: 9/8*): 2.22, 2.23, 2.27, 2.41, 2.43

9/3/2010 (*Due: 9/8*): 4.6, 4.7  
*Total possible points = 65*

9/6/2010: no class, now hwk  
9/8/2010 (*Due: 9/15*): 4.13, 4.16, 4.17, 4.19. 4.20  
9/10/2010 (*Due: 9/15*): 4.21, 4.22, 4.33  
*Total possible points = 40*  
9/13/2010: review, no hwk

9/15/2010 (*Due: 9/29/2010*): 5.1. Convert 45610 and 65310 to binary representation. Convert (10100010)2 and (01110001)2 to decimal, hexadecimal, and octal representations.

9/17/2010 (*Due: 9/29/2010*): 5.2, 5.3, 5.4

9/20/2010 (*Due: 9/29/2010*): 5.5, Describe the differences of half-adder and full-adder. Why 2’s complement is more suitable for arithmetic operations than 1’s complement and sign-magnitude?

9/22/2010: no hwk, test 1  
9/24/2010 (*Due: 9/29/2010*):: 5.7, Design an 8-bit adder/subtractor using the one-bit FA.

9/27/2010 (*Due: 10/6/2010*): 5.12, 5.13, 5.14, 5.21  
9/29/2010 (*Due: 10/6/2010*): 6.1, 6.2, 6.4. 6.5, 6.6  
10/1/2010 (*Due: 10/6/2010*): 6.11, 6.16, 6.17  
10/4/2010 (*Due: 10/13/2010*): 6.29, 6.30  
10/6/2010 (*Due: 10/13/2010*): 7.1, 7.3  
10/8/2010 (*Due: 10/13/2010*): 7.31, What is the difference between D latch and D flip-flop? What is the difference between logic gates (e.g. AND, OR, NOT, XOR, NAND, NOR) and D latch?  
10/11/2010 (*Due: 10/20/2010*): Design a 3-bit “counter” with this output sequence (000After 111, the sequence will restart at 000.  
10/13/2010 (*Due: 10/20/2010*): Design a 3-bit up/down counter.  
10/15/2010 (*Due: 10/20/2010*): no hwk

10/18/2010 (*Due: 10/27/2010*): Design a “10” sequence detector. Show your state diagram state table, decoded state table (using minimized-bit encoding, and logic circuit. Re-do with one-hot encoding.

10/20/2010 (*Due: 10/27/2010*): Design a sequence detector for detecting “1001.” Use minimized bit encoding. Solve the problem with Moore and Mealy.

10/22/2010 (*Due: 10/27/2010*): Simulate the hwk assigned on 10/18 and 10/20. As part of the hwk submission, print the logic schematics diagrams and simulation waveforms. For 10/18, you only need to simulate the minimized-bit encoding version.  
10/25/2010 (*Due: 11/3/2010*): 8.3, 8.9

10/27/2010 (*Due: 11/3/2010*): Given *f = wx + yz*. Implement *f* using AND, OR, and NOT gates. What is your transistor count?  Re-implement  *f* using NAND gates. Again, re-implement *f* using NOR gates. What are your transistors count? For all three cases, show your transistors diagrams of *f*.

10/29/2010 (*Due: 11/3/2010*): no hwk

11/1/2010 – 11/5/2010: Review, Test II, Test Review

11/8/2010 (Due: 11/17/2010): 8.20, 8.21

11/10/2010 (Due: 11/17/2010): 8.23, 8.24, 8.26

11/12/2010 (Due: 11/17/2010): 9.10, 9.11

11/15/2010 (Due: 12/1/2010): 8.11, 8.37

11/17/2010 (Due: 12/1/2010): 8.15, 16

11/19/2010 (Due: 12/1/2010): 8.14